WE CLAIM:

1. A copper interconnect structure, comprising:

a semiconductor substrate;

a dielectric layer over said semiconductor substrate;

a trench in said dielectric layer;

a barrier layer in said trench wherein said barrier layer comprises a material from the group consisting of iridium (Ir), ruthenium (Ru), rhodium (Rh), rhenium (Re), platinum (Pt), and palladium (pd); and

copper filling said trench over said barrier layer.

2. The copper interconnect structure of claim 1 further comprising;

a via in said dielectric layer;

a trench in said dielectric layer;

a barrier layer in said via wherein said barrier layer comprises a material from the group consisting of iridium (Ir), ruthenium (Ru), rhodium (Rh), rhenium (Re), platinum (Pt), and palladium (pd); and

copper filling said via over said barrier layer.

3. The copper interconnect structure of claim 2 wherein said via is positioned beneath said trench.

4. A copper interconnect structure, comprising:

a semiconductor substrate;

a dielectric layer over said semiconductor substrate;

a trench in said dielectric layer;

a first barrier layer in said trench wherein said barrier layer comprises a material from the group consisting of iridium oxide, ruthenium oxide, rhodium oxide, rhenium oxide, platinum oxide, and palladium oxide; and

copper filling said trench over said barrier layer.

5. The copper interconnect structure of claim 4 further comprising;

a via in said dielectric layer;

a trench in said dielectric layer;

a first barrier layer in said via wherein said first barrier layer comprises a material from the group consisting of iridium oxide, ruthenium oxide, rhodium oxide, rhenium oxide, platinum oxide, and palladium oxide; and

copper filling said via over said barrier layer.

6. The copper interconnect structure of claim 5 wherein said via is positioned beneath said trench.

7. The copper interconnect of claim 6 further comprising a second barrier layer wherein said second barrier layer comprises a material selected from the group consisting of iridium (Ir), ruthenium (Ru), rhodium (Rh), rhenium (Re), platinum (Pt), and palladium (pd).

8. A method for forming a copper interconnect structure, comprising:

forming a dielectric layer over a semiconductor substrate;

forming a trench in said dielectric layer;

forming a via in said trench;

deposition a first barrier layer in said trench and via wherein said first barrier layer comprises a material selected from the group consisting of iridium (Ir), ruthenium (Ru), rhodium (Rh), rhenium (Re), platinum (Pt), and palladium (pd); and

filling said trench and said via with copper formed over said first barrier layer.

9. The method of claim 8 further comprising forming a second barrier layer beneath said copper wherein said second barrier layer comprises a material selected from the group consisting of iridium oxide, ruthenium oxide, rhodium oxide, rhenium oxide, platinum oxide, and palladium oxide.

10. A method for forming an integrated circuit with copper interconnects, comprising:

forming a dielectric layer over a semiconductor substrate;

forming a trench in said dielectric layer;

forming a via in said trench;

deposition a first barrier layer in said trench and via wherein said first barrier layer comprises a material selected from the group consisting of iridium oxide, ruthenium oxide, rhodium oxide, rhenium oxide, platinum oxide, and palladium oxide; and

filling said trench and said via with copper formed over said first barrier layer.